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[on](#)
 11-13 Oct. 2004 Page(s):288 - 294
 Digital Object Identifier 10.1109/ICCD.2004.1347935
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 Raasch, S.E.; Reinhardt, S.K.;
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 27 Sept.-1 Oct. 2003 Page(s):15 - 25
 Digital Object Identifier 10.1109/PACT.2003.1237998
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 Oberoi, P.S.; Sohi, G.S.;
[Computer Architecture, 2003. Proceedings. 30th Annual International Symposium on](#)
 9-11 June 2003 Page(s):230 - 240
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 Reaz, M.B.I.; Islam, M.S.; Sulaiman, M.S.;
[Semiconductor Electronics, 2002. Proceedings. ICSE 2002. IEEE International Conference on](#)
 19-21 Dec. 2002 Page(s):199 - 203
[AbstractPlus](#) | Full Text: [PDF](#)(376 KB) IEEE CNF
[Rights and Permissions](#)
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 Won-Kee Hong; Seung-Yup Lee; Shin-Dug Kim;
[ASICs, 1999. AP-ASIC '99. The First IEEE Asia Pacific Conference on](#)
 23-25 Aug. 1999 Page(s):95 - 98
 Digital Object Identifier 10.1109/APASIC.1999.824037

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6. A low-cost VLIW DSP architecture for communication equipment

Petit, L.; Legat, J.-D.;

[Signals, Systems, and Electronics, 1998. ISSSE 98. 1998 URSI International Symposium on](#)
29 Sept.-2 Oct. 1998 Page(s):278 - 281

Digital Object Identifier 10.1109/ISSSE.1998.738081

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7. Aggressive dynamic execution of multimedia kernel traces

Bishop, B.; Owens, R.; Irwin, M.J.;

[Parallel Processing Symposium, 1998. 1998 IPPS/SPDP. Proceedings of the First Merged Internal Symposium on Parallel and Distributed Processing 1998](#)

30 March-3 April 1998 Page(s):640 - 646

Digital Object Identifier 10.1109/IPPS.1998.669994

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8. Instruction set architecture of an efficient pipelined dataflow architecture

Gao, G.R.; Tio, R.;

[System Sciences, 1989. Vol.1: Architecture Track. Proceedings of the Twenty-Second Annual Hawaii Conference on](#)

Volume 1, 3-6 Jan. 1989 Page(s):385 - 392 vol.1

Digital Object Identifier 10.1109/HICSS.1989.47180

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